



- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

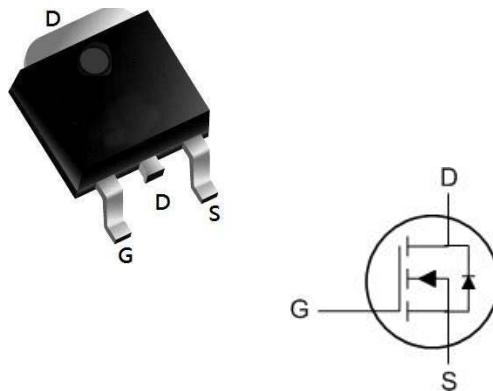
BVDSS	RDS(on)	ID
100V	65mΩ	20A

Description

The XXW20N10 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The XXW20N10 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	20	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	12	A
I _{DM}	Pulsed Drain Current ²	80	A
EAS	Single Pulse Avalanche Energy ³	4.1	mJ
I _{AS}	Avalanche Current	10	A
P _D @T _C =25°C	Total Power Dissipation ³	41.7	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	50	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	3.0	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current $T_J=25^\circ\text{C}$ $T_J=100^\circ\text{C}$	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA
			-	-	100	
Gate-Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.2	-	2.5	V
Drain-Source on-Resistance ⁴	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 5\text{A}$	-	65	90	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 3\text{A}$	-	75	105	
Forward Transconductance ⁴	g_{fs}	$V_{\text{DS}} = 5\text{V}, I_D = 5\text{A}$	-	12	-	S
Dynamic Characteristics⁵						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$	-	1220	-	pF
Output Capacitance	C_{oss}		-	53	-	
Reverse Transfer Capacitance	C_{rss}		-	42	-	
Gate Resistance	R_g	$f = 1\text{MHz}$	-	1.3	-	Ω
Switching Characteristics⁵						
Total Gate Charge	Q_g	$V_{\text{GS}} = 10\text{V}, V_{\text{DS}} = 50\text{V}, I_D = 5\text{A}$	-	20.6	-	nC
Gate-Source Charge	Q_{gs}		-	4	-	
Gate-Drain Charge	Q_{gd}		-	3.7	-	
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, V_{\text{DD}} = 50\text{V}, R_G = 3\Omega, I_D = 5\text{A}$	-	4.7	-	ns
Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	20	-	
Fall Time	t_f		-	16	-	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ⁴	V_{SD}	$I_S = 1\text{A}, V_{\text{GS}} = 0\text{V}$	-	-	1.2	V
Continuous Source Current	$T_C = 25^\circ\text{C}$	I_S	-	-	20	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})} = 150^\circ\text{C}$.
2. The data tested by pulsed, pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{\text{DD}} = 25\text{V}, V_{\text{GS}} = 10\text{V}, L = 0.1\text{mH}, I_{\text{AS}} = 8\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

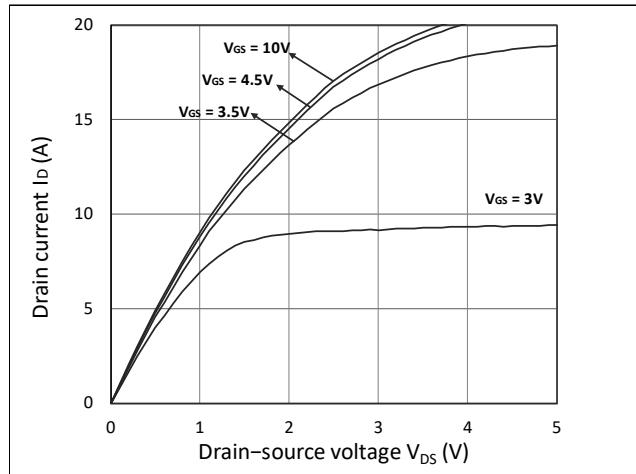


Figure 1. Output Characteristics

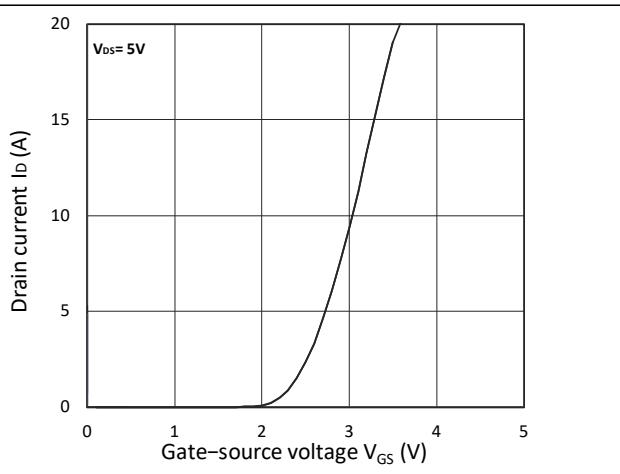


Figure 2. Transfer Characteristics

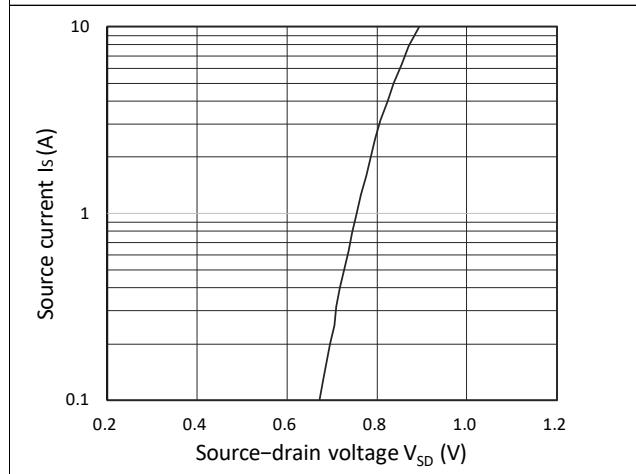
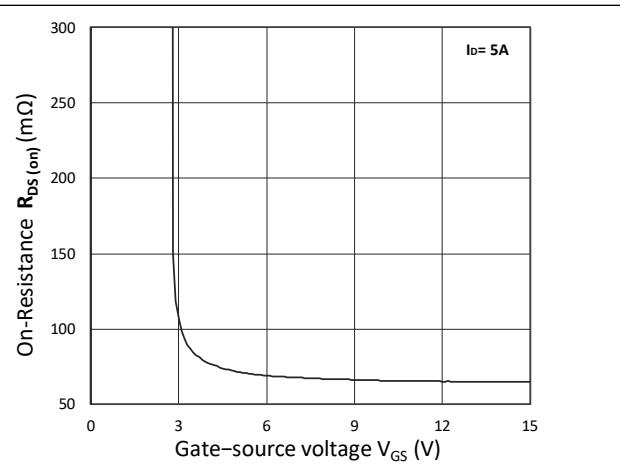
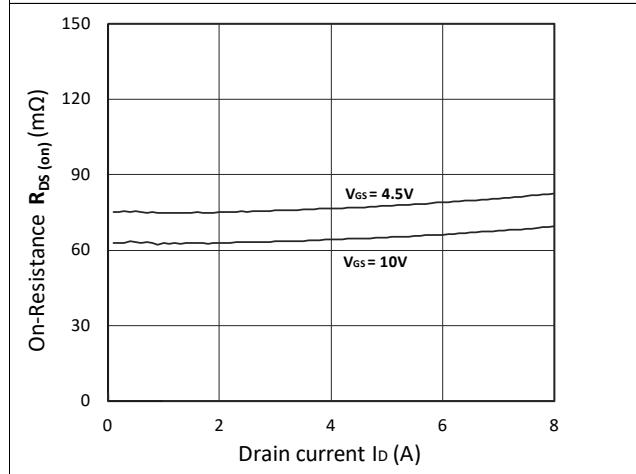
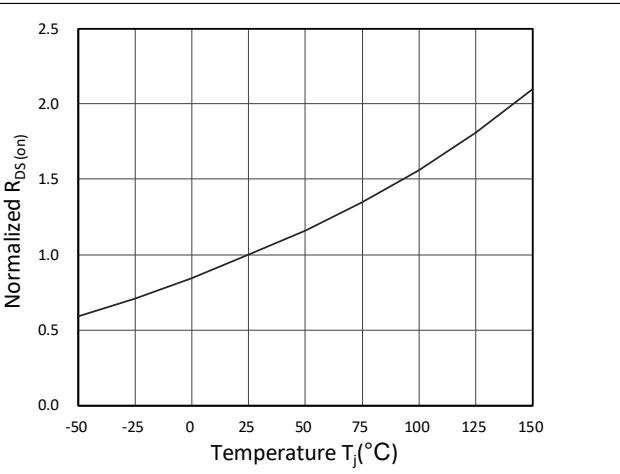


Figure 3. Forward Characteristics of Reverse


 Figure 4. $R_{DS(on)}$ vs. V_{GS}

 Figure 5. $R_{DS(on)}$ vs. I_D

 Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

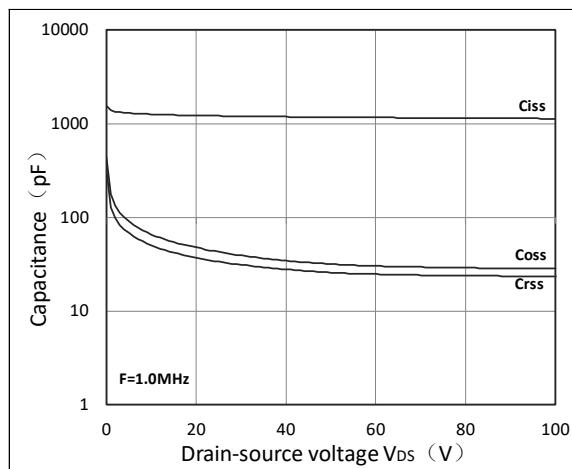


Figure 7. Capacitance Characteristics

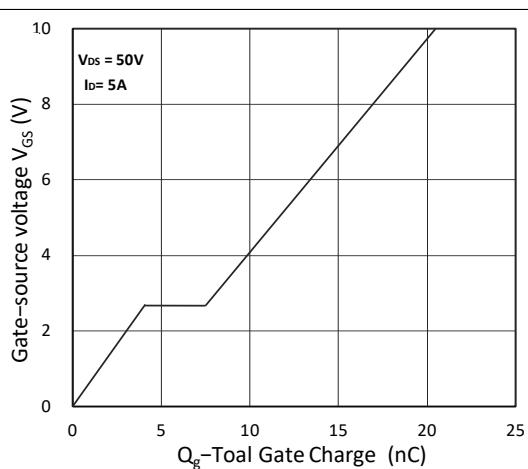


Figure 8. Gate Charge Characteristics

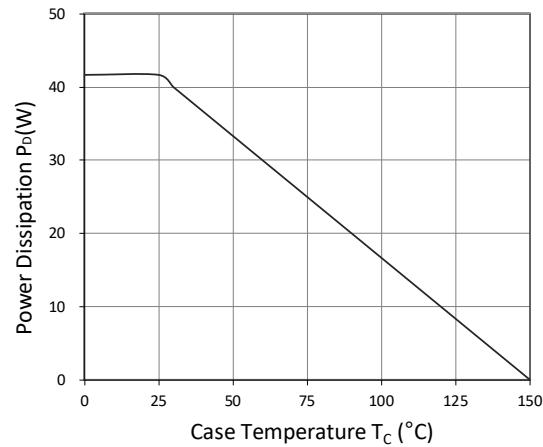


Figure 9. Power Dissipation

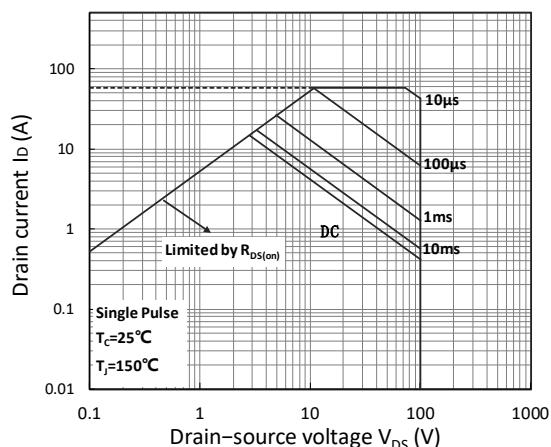


Figure 10. Safe Operating Area

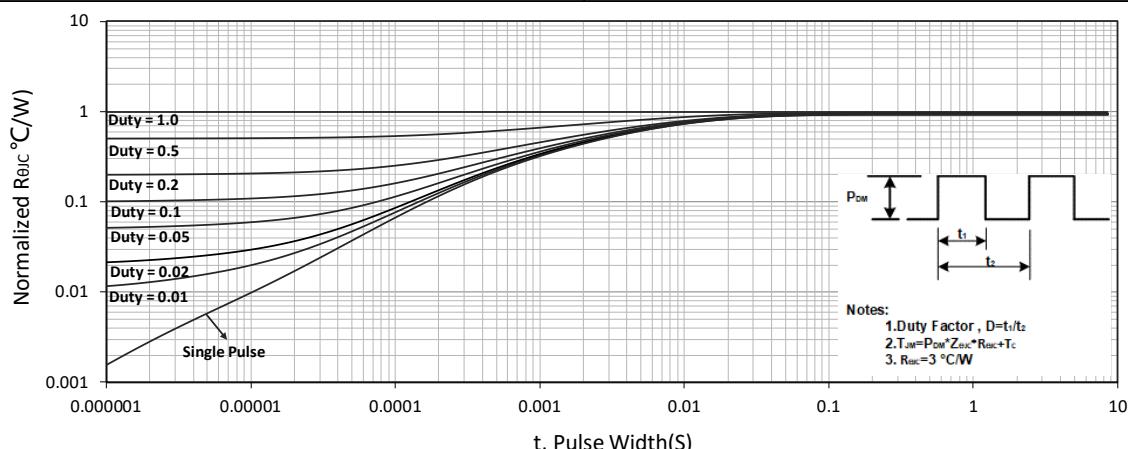
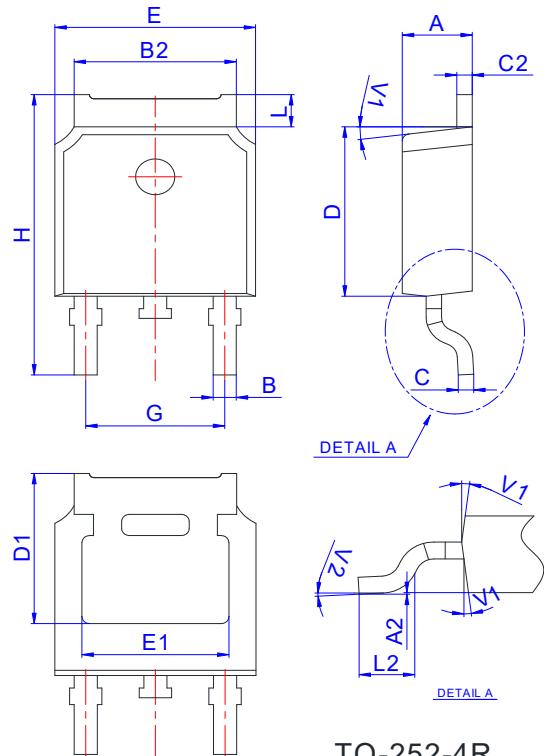


Figure 11. Normalized Maximum Transient Thermal Impedance

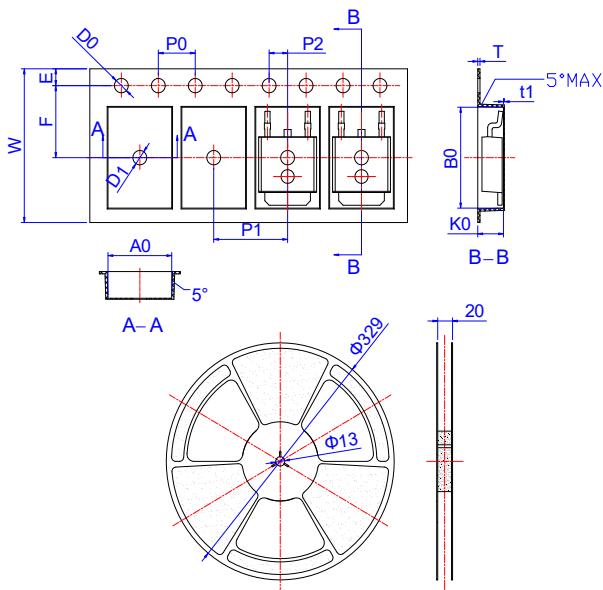
TO-252 Package outline



TO-252-4R

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583