

Features

- 100V, 75A
- $R_{DS(ON)} < 9.2\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 13.5\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired



Product Summary

BVDSS	RDS(on)	ID
100V	7.3 mΩ	75 A

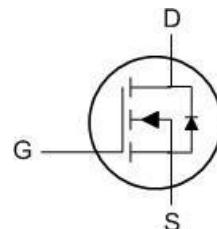
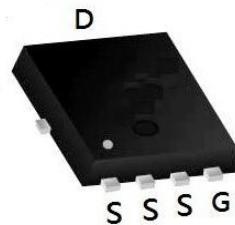
PRPAK5X6 Pin Configuration

Application

- Load Switch
- PWM Application
- Power management

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Absolute Maximum Ratings

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	75	A
		$T_C = 100^\circ\text{C}$	49	A
I_{DM}	Pulsed Drain Current ^{note1}		300	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		90	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	97	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.3	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=100\text{V}$, $V_{\text{GS}}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}= \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=250\mu\text{A}$	1.0	1.6	2.5	V
$R_{\text{DS}(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	-	7.3	9.2	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=8\text{A}$	-	9	13.5	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=50\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1.0\text{MHz}$	-	2046	-	pF
C_{oss}	Output Capacitance		-	865	-	pF
C_{rss}	Reverse Transfer Capacitance		-	25	-	pF
Q_g	Total Gate Charge	$V_{\text{DS}}=50\text{V}$, $I_D=30\text{A}$, $V_{\text{GS}}=10\text{V}$	-	39.4	-	nC
Q_{gs}	Gate-Source Charge		-	5.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	9.8	-	nC
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DD}}=50\text{V}$, $I_D=25\text{A}$, $R_G=6\Omega$, $V_{\text{GS}}=10\text{V}$	-	20	-	ns
t_r	Turn-on Rise Time		-	5.2	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	49	-	ns
t_f	Turn-off Fall Time		-	12	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	75	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	300	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=30\text{A}$	-	-	1	V
t_{rr}	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}$, $I_F=12\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	49	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	85	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{\text{DD}}=50\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{\text{AS}}=19\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

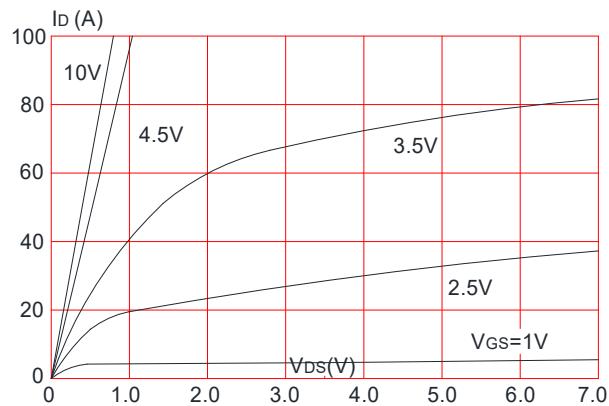


Figure 3: On-resistance vs. Drain Current

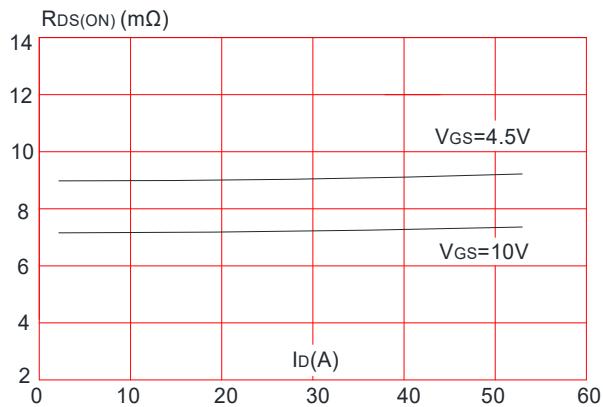


Figure 5: Gate Charge Characteristics

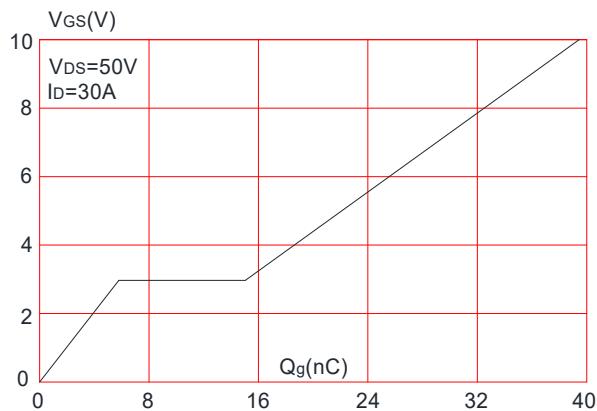


Figure 2: Typical Transfer Characteristics

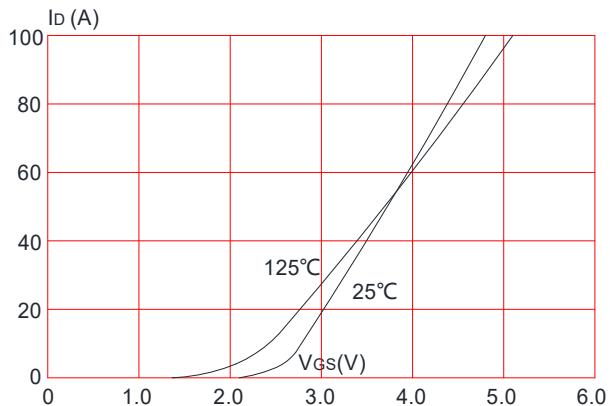


Figure 4: Body Diode Characteristics

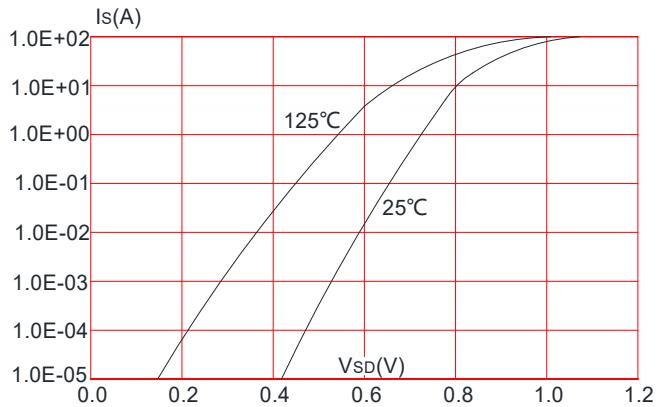
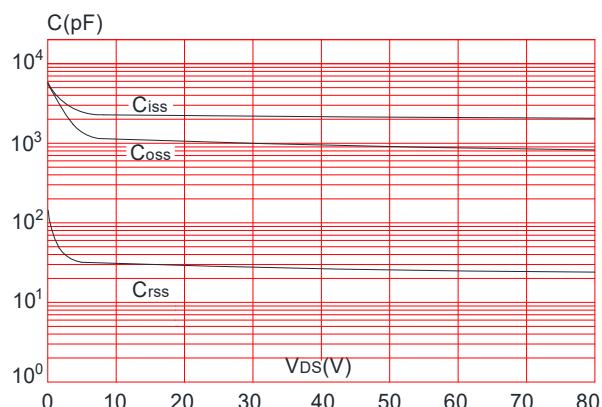


Figure 6: Capacitance Characteristics



N-Ch 100V Fast Switching MOSFETs

Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

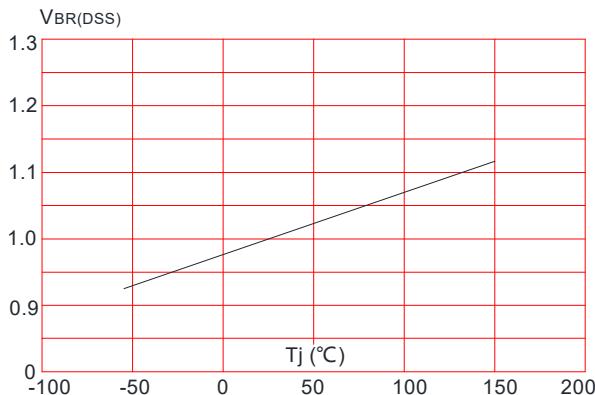


Figure 8: Normalized on Resistance vs. Junction Temperature

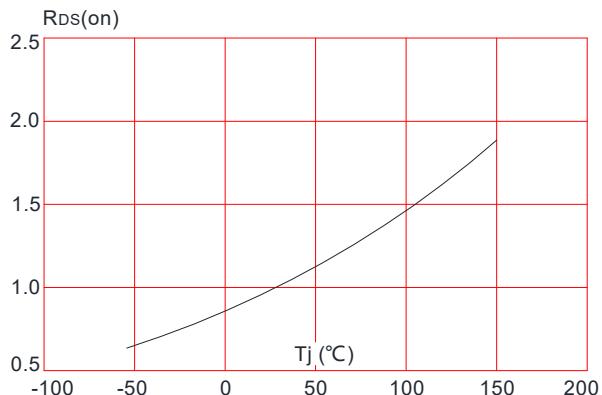


Figure 9: Maximum Safe Operating Area

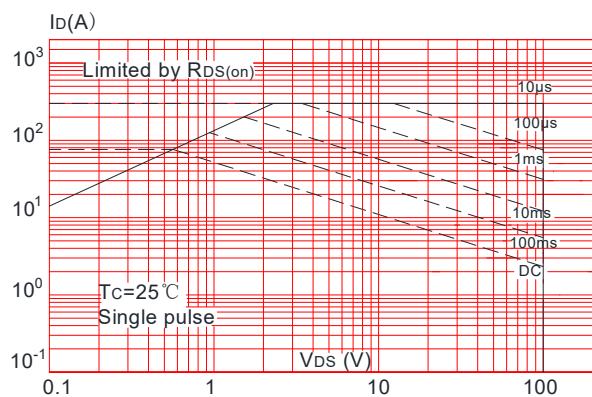


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

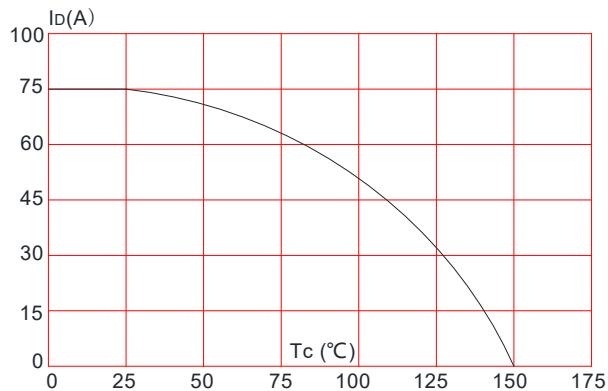
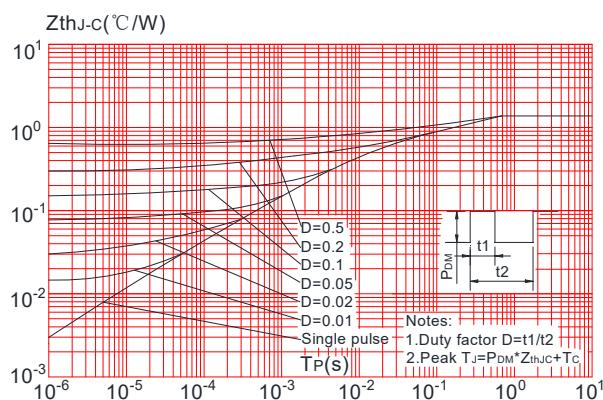


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

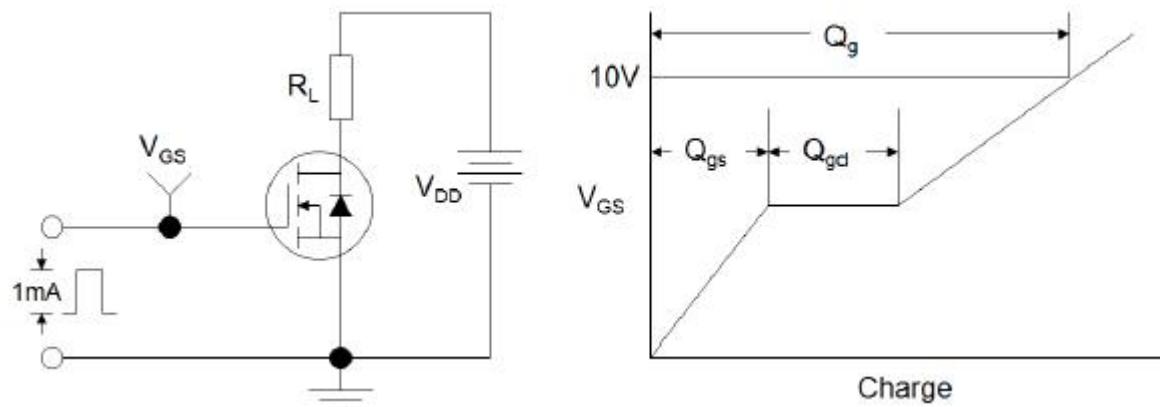


Figure 1: Gate Charge Test Circuit & Waveform

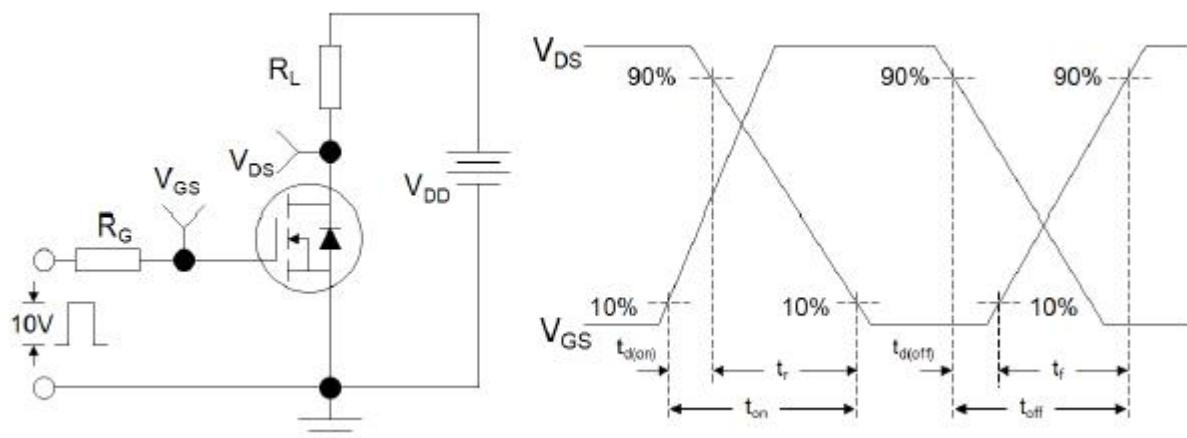


Figure 2: Resistive Switching Test Circuit & Waveforms

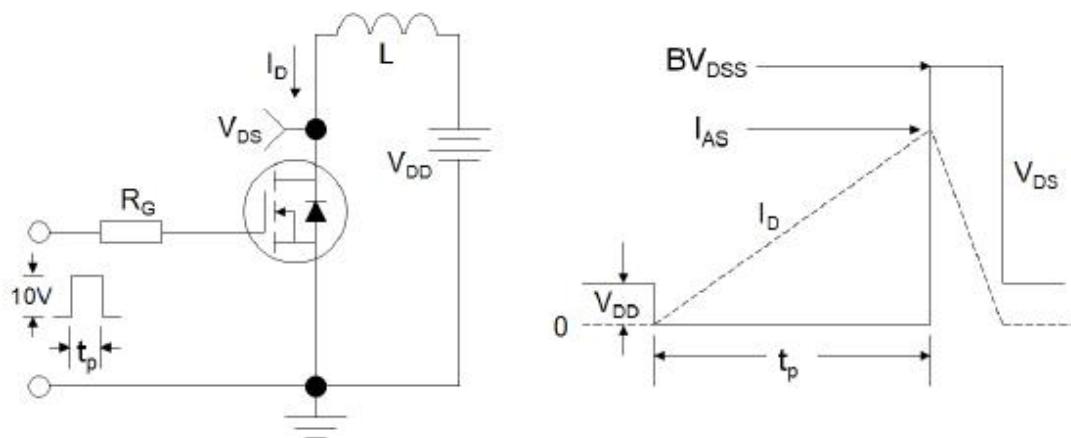
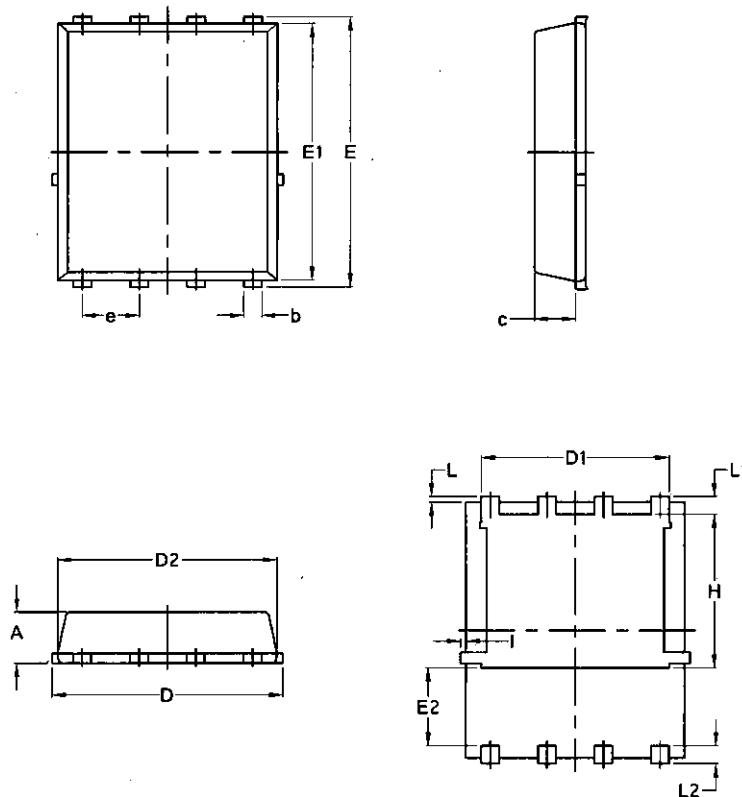


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-PDFN5*6-8L- Single


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070